

The diagram illustrates the system architecture of the AD9100 microprocessor. At the top center is the **AD9100 Microprocessor 105**, which includes a **Cache + Protection Unit** (Unified Code/Data, 8KBytes, 512 Lines, 4 way set assoc) and is connected to a **Local CPU Bus 145**. To the left of the bus are the **JTAG Unit 135** and **Breakpoint Unit 150**. To the right are the **Core Interface Unit** and **16KBytes ScratchPad SRAM 145**. A **DMA Controller 4 independent DMA channels 145** is also connected to the bus. A **Configurable System Interconnect Bus 115** runs horizontally across the middle. Below it is the **Local Interface Unit**, which contains **ROM**, **Control registers**, **Memory Interface Unit (FLASH, SDRAM) 140**, and a **Configuration Unit**. The **Configuration Unit** is connected to the **Configurable System Logic 120**, which in turn connects to **Programmable IOs 125**. A **Peripheral 130** block (containing 2 Timers, Interrupt ctrl, 2 UARTs, Watchdog) and a **Clock Generation Reset Control Power Management** block are also shown. An **External FLASH Bypass** path is indicated from the bus to the Memory Interface Unit. A **CSI Arbiter** is shown at the top right.

Figure 1

Reset the device ~ 205

Execute from internal ROM
and search for valid secondary
initialization code in external
memory ~ 210

Branch to ROM at
the top of memory ~ 215

Disable ROM alias ~ 220

Jump to secondary initialization
routine ~ 225

Configure the device ~ 230

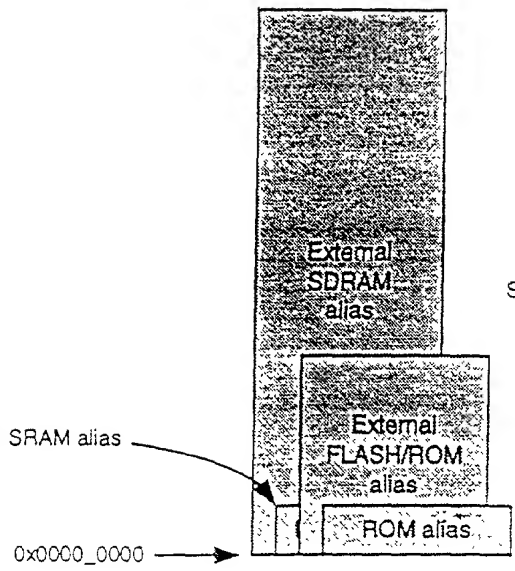
Reset the CPU ~ 235

Start executing from the
bottom of external memory ~ 240

Set up the application program ~ 245

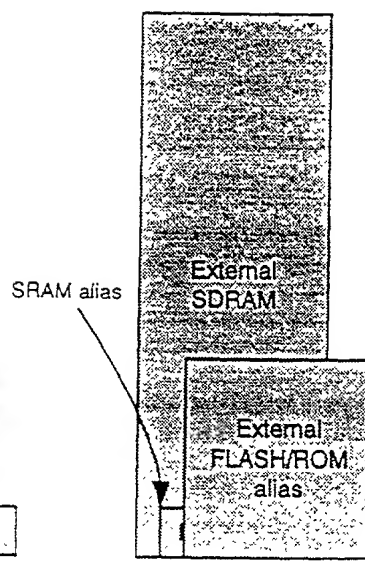
Disable the external memory
alias ~ 250

Figure 2



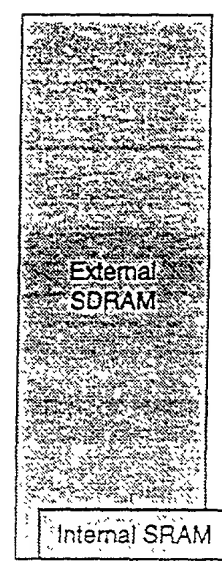
Device
Configuration
Phase

Figure 3A



Disal Com
Secondary
Configuration
and
Start of Application

Figure 3B



Normal
Operation
Mode

Figure 3C